4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,508	10/06/2003	Darrell Rinerson	UNTYP022	5040

42958 7590 11/16/2004

UNITY SEMICONDUCTOR CORPORATION
250 NORTH WOLFE ROAD
SUNNYVALE, CA 94085

EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/680,508	**Applicant(s)** RINERSON ET AL.	
	Examiner Gene N Auduong	**Art Unit** 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-38_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-38_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _01-26-04 &02-27-04_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on January 26, 2004 and February 27, 2004 is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-38 are rejected under 35 U.S.C. 102(a) as being anticipated by Moore et al. (U.S. Pat No. 6,515,904).

Regarding claim 1, Moore et al. disclose a program circuit for a programming a selected cell to a desired resistive state in a conductive re-writable memory comprising: a first reference input (figures 2 and 3, reference voltage Vref); a selected cell input from the selected cell, the selected cell having a resistance (non-volatile memory can be type of memory cell; col. 2, line 23+), the resistance capable of representing stored information (data value in the memory cell representing stored information); and a first comparator (figure 2, comparator 130; figure 3, comparator 150) that is capable of producing a first comparator output that is a function of the selected cell input and the first reference input (comparator 150 outputting a signal that is function of the selected cell input and the reference input).

Regarding claim 2, Moore et al. disclose the program circuit of claim 1, wherein the function is a direct comparison of the selected cell input and the first reference input (output of the comparator 130 or 150 is comparing the reference input and the selected cell).

Regarding claim 3, Moore et al. disclose the program circuit of claim 2, wherein the direct comparison is a comparison of: voltage from the selected cell input and voltage of the first reference input; or current from the selected cell input and current of the first reference input; or resistance from the selected cell input and resistance of the first reference input (col. 4, lines 24+).

Regarding claim 4, Moore et al. disclose the program circuit of claim 2, wherein: the comparator output causes the program circuit to cease programming when the selected cell input equals the first reference input (col. 4, lines 13+).

Regarding claim 5, Moore et al. disclose the program circuit of claim 4, wherein: the resistance is capable of representing more than one bit of information (non-volatile memory cell type can be single bit or multiple bit; col. 2, line 45+).

Regarding claim 6, Moore et al. disclose the program circuit of claim 1, further comprising: a second reference input (figure 2); and a second comparator that is capable of producing a second comparator output that is a function of the selected cell input and the second reference input (figure 2).

Regarding claim 7, Moore et al. disclose the program circuit of claim 6, wherein: the programming of the selected cell is dependent upon either the first comparator output or the second comparator output, depending on the desired state to be programmed into the selected cell (col. 4, lines 1+).

Regarding claims 8-9, Moore et al. disclose the program circuit of claim 7, wherein: if the programming of the selected cell is dependent upon the first comparator output, the first comparator output can cause the programming circuit to cease programming; and if the programming of the selected cell is dependent upon the second comparator output, the second comparator output can cause the programming circuit to cease programming; wherein: the first comparator output causes the program circuit to cease programming when the selected cell input is equivalent to the first reference input; and the second comparator output causes the program circuit to cease programming when the selected cell input is equivalent to the second reference input (col. 4, lines 1+).

Regarding claim 10, Moore et al. disclose the program circuit of claim 6, further comprising: a first load circuit coupled to the selected cell; a second load circuit that receives the first reference input; a third load circuit that receives the second reference input; wherein the first, second and third load circuits have essentially the same load characteristics (figure 2, col. 4, lines 1+).

Regarding claim 11, Moore et al. disclose the program circuit of claim 6, wherein: the first comparator and the second comparator are voltage comparators (comparators 130 and 150 receiving the reference voltage, inherently, they are voltage comparators).

Regarding claim 12, Moore et al. disclose the program circuit of claim 6, wherein: the first comparator output and the second comparator output are combined, the programming of the selected cell being dependent upon the combination (col. 4, lines 1+).

Regarding claim 13, Moore et al. disclose the program circuit of claim 1, wherein: the comparator output is bypassed during an initialization step (does not shown, inherently, comparator output is bypass due to non of the memory cell is being write or read).

Claims 14-38 contain the similar limitation as previously discussed in claims 1-13 but claiming in the alternative way. Therefore, they are analyzed as previously discussed with respect to claims 1-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
November 11, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818